Description

METHOD FOR FABRICATING A TRENCH CAPACITOR

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a semiconductor process, and more particularly, to a process of manufacturing a deep trench capacitor of a DRAM device.

[0003] 2. Description of the Prior Art

[0004] Trench-capacitor DRAM devices are known in the art. A trench-storage capacitor typically consists of a very-high-aspect-ratio contact-style hole pattern etched into the substrate, a thin storage-node dielectric insulator, a doped low-pressure chemical vapor deposition (LPCVD) polysilicon fill, and buried-plate diffusion in the substrate. The doped LPCVD silicon fill and the buried plate serve as the electrodes of the capacitor. A dielectric isolation collar in the upper region of the trench prevents leakage of the

signal charge from the storage-node diffusion to the buried-plate diffusion of the capacitor.

[0005] In general, the prior art method for fabricating a trench capacitor of a DRAM device may include several major manufacture phases as follows:

[0006] Phase 1: deep trench etching.

[0007] Phase 2: buried plate and capacitor dielectric (or node di-electric) forming.

[0008] Phase 3: first polysilicon deep trench fill and first recess etching.

[0009] Phase 4: collar oxide forming.

[0010] Phase 5: second polysilicon deposition and second recess etching.

[0011] Phase 6: collar oxide wet etching.

[0012] Phase 7: third polysilicon deposition and third recess etching.

[0013] Phase 8: shallow trench isolation (hereinafter referred to as "STI") forming.

[0014] Please refer to Fig.1 and Fig.2. Fig.1 and Fig.2 are schematic cross-sectional diagrams showing several in-termediate steps of forming a prior art deep trench ca-pacitor, which are relative to the present invention. As

shown in Fig.1, a substrate 10 having a pad oxide layer 26 and a pad nitride layer 28 thereon is provided. After deep trench etching, an N^+ buried plate 13 and a node dielectric layer 14 are sequentially formed in the deep trench. A first polysilicon deposition and recess process is then carried out to form a first poly layer (Poly1) at the bottom of the deep trench. A collar oxide layer 15 is formed on sidewall of the deep trench above Poly1. A second polysilicon deposition and recess process is then carried out to form a second poly layer (Poly2) atopPoly1. The collar oxide layer 15 that is not covered by Poly 2 is stripped off to expose the sidewall of the deep trench. Subsequently, as shown in Fig.2,a third polysilicon deposition and recess process is carried out to form a third poly layer (Poly3) atopPoly2 and collar oxide layer 15. Dopants of the heavily doped Poly2 diffuse out through Poly3 to the surrounding substrate 10 to form an annular shaped buried strap out diffusion regions 16 in the following thermal process. A conventional STI process is performed to isolate the two adjacent deep trench capacitors.

[0015] Please refer to Fig.3. Fig.3 is an enlarged schematic plane view showing the layout of the memory chip containing the trench capacitors made according to the prior art

method as set forth in Fig.1 and Fig.2. The perspective buried strap out diffusion regions 16 encircling each of the trench capacitors 11 are also illustrated in Fig.3, which are indicated with dash lines. As shown in Fig.3, to achieve a maximum packing density, pairs of trench capacitors are arranged in very close distance.

[0016] Please refer to Fig.4 to Fig.6. Fig.4 is an enlarged schematic plane view showing, in an ideal condition, the layout of the deep trench (DT) capacitors 11 and active area photoresist (AA photo) pattern without AA-DT misalignment. Fig.5 is a schematic cross-sectional diagram showing the deep trench capacitor 11 and the AA photo along line NN" of Fig.4, before STI etching. Fig.6 is a schematic cross-sectional diagram showing the deep trench capacitor 11 and the shallow trench isolation (STI) along line NN" of Fig.4. As shown in Fig.4 and Fig.5, in an ideal condition, the AA photo that is used to define active areas on the substrate and to define isolation shallow trenches to be etched into the substrate does not overlap with the annular buried strap out diffusion regions 16. As shown in Fig.5, the AA photo is typically patterned on an intermediate dielectric layer such as a BSG layer using lithographic process known in the art. Using the AA photo

and the BSG layer as an etching hard mask, STI trenches are etched into the substrate that is not masked by the AA photo pattern using dry etching such as RIE. After removing the remaining photoresist and BSG layer, STI fill material such as high-density plasma chemical vapor deposition (HDPCVD) oxide is then deposited into the STI trenches, followed by CMP planarization, thereby forming the structure as set forth in Fig.6. It is noted that since the AA photo does not overlap with the buried strap out diffusion region of a neighboring deep trench capacitor in y direction, most of the buried strap out diffusion region surrounding the deep trench capacitor is etched away during the above-said STI process.

[0017]   Please refer to Fig.7 and Fig.8. Fig.7 is an enlarged schematic plane view showing, in a non-ideal condition, the layout of the deep trench (DT) capacitors 11 and active area photoresist (AA photo) pattern with AA-DT misalignment. Fig.8 is a schematic cross-sectional diagram showing the deep trench capacitor 11 and the AA photo along line NN" of Fig.7. In practice, misalignment between the AA photo and the deep trench capacitors 11 usually occurs. As shown in Fig.7, the AA photo shifts a distance in y direction. This causes AA photo to overlap with the

buried strap out diffusion regions 16 of neighboring deep trench capacitors. As shown in Fig.8, after STI formation, the masked buried strap out diffusion region 16, which is not etched away during the STI process, will adversely affect the active areas and transistor characteristics.

SUMMARY OF INVENTION

[0018] Accordingly, the primary object of the present invention is to provide a method for fabricating a deep trench capacitor and trench capacitor memory devices, which is capable of avoiding the above-mentioned problems.

[0019] According to the claimed invention, a method for fabricating a trench capacitor is disclosed. A substrate having a deep trench etched therein is provided. The deep trench is then doped to form a buried plate electrode in the substrate adjacent to a lower portion of the deep trench. A node dielectric layer is formed on interior surface of the deep trench. A first conductive layer is thereafter deposited in the deep trench. The first conductive layer is then recessed to a first depth in the deep trench. A collar oxide layer is formed on sidewall of the deep trench above the first conductive layer. A second conductive layer is deposited on the first conductive layer and the collar oxide layer. The second conductive layer is recessed to a second

depth inside the deep trench. A pair of symmetric spacers is formed on sidewall of the deep trench above the second conductive layer in a first direction and exposing a silicon sidewall of the deep trench above the second conductive layer in a second direction, wherein the first direction is substantially orthogonal to the second direction. A third conductive layer is then deposited on the second conductive layer and on the spacers, and recessed to a third depth inside the deep trench.

[0020] It is to be understood that both the foregoing general description and the following detailed description are exemplary, but are not restrictive, of the invention. Other objects, advantages, and novel features of the claimed invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0021] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

[0022] Fig.1 and Fig.2 are schematic cross-sectional diagrams showing several intermediate steps of forming a prior art deep trench capacitor (before STI process), which are relative to the present invention;

[0023] Fig.3 is an enlarged schematic plane view showing the layout on the memory chip containing the trench capacitors made according to the prior art method as set forth in Fig.1 and Fig.2;

[0024] Fig.4 is an enlarged schematic plane view showing, in an ideal condition, the layout of the deep trench (DT) capacitors and active area photoresist (AA photo) pattern without AA-DT misalignment;

[0025] Fig.5 is a schematic cross-sectional diagram showing the deep trench capacitor and the AA photo along line NN" of Fig.4;

[0026] Fig.6 is a schematic cross-sectional diagram showing the deep trench capacitor and the shallow trench isolation (STI) along line NN" of Fig.4;

[0027] Fig.7 is an enlarged schematic plane view showing, in a non-ideal condition, the layout of the deep trench (DT) capacitors and AA photo pattern with AA-DT misalignment;

[0028] Fig.8 is a schematic cross-sectional diagram showing the

deep trench capacitor and the AA photo along line NN" of Fig.7 (after STI process);

[0029] Fig.9 to Fig.14 are schematic cross-sectional diagrams illustrating the method for fabricating deep trench capacitor according to the preferred embodiment of the present invention; and

[0030] Fig.15 is a schematic plane view showing the layout of the deep trench capacitors after finishing the process steps through Fig.9 to Fig.14 and buried strap out diffusion process, wherein the perspective non-circular buried strap out diffusion regions 16 are also shown.

DETAILED DESCRIPTION

[0031] Please refer to Fig.9 to Fig.14. Fig.9 to Fig.14 are schematic cross-sectional diagrams illustrating the method for fabricating deep trench capacitor according to the preferred embodiment of the present invention. As shown in Fig.9, a semiconductor substrate 10 such as a silicon substrate is provided. A pad oxide layer 26 and a pad nitride layer 28 are formed on a surface of the semiconductor substrate 10. A deep trench etching is then carried out to form a deep trench in the substrate 10. The formation of a deep trench in a silicon substrate is known in the art. A dry etching process such as RIE is typically

used to form a deep trench in the semiconductor sub-strate 10. A buried plate 13 adjacent to the deep trench and a node dielectric layer 14 are formed. A first polysilicon deposition and recess process is carried out to form a first poly layer (Poly1) inside the deep trench. A collar oxide layer 15 is formed on sidewall of the deep trench above Poly1. A second polysilicon deposition and recess process is then carried out to form a second poly layer (Poly2) atopPoly1 and collar oxide. The method of forming the buried plate 13 comprises the steps of depositing a thin layer of arsenic silicate glass (ASG) at a lower portion of the deep trench, followed by thermal drive in. It is understood that other doping methods such as gas phase doping (GPD) or the like may be employed. The node dielectric layer 14 may be oxide-nitride (ON) or oxide-nitride-oxide (ONO), but not limited thereto. After performing the second polysilicon deposition and recess process, the trench sidewall, the top surface of Poly2 and the exposed surface of the collar oxide layer 15 define a recess at the top of the deep trench.

[0032] Still referring to Fig.9, a top view of the oval shaped deep trench capacitor is also illustrated at the lower portion of Fig.9. Subsequently, a thin silicon oxide layer 31 is de-

posited on interior surface of the recess at the top of the deep trench, i.e., on the exposed trench sidewall, the exposed top surface of the collar oxide 15, and the top surface of Poly2. The conformal silicon oxide layer 31 also covers the pad nitride layer 28 and the exposed pad oxide layer 26. Preferably, the thin silicon oxide layer 31 is deposited using chemical vapor deposition (CVD) method and has a thickness of about 100~200 angstroms, preferably 150 angstroms. An amorphous silicon film 32 is then deposited on the conformal silicon oxide layer 31. The amorphous silicon film 32 has a thickness of about 50 angstroms.

[0033] As shown in Fig.10, a tilt angle ion implantation process is carried out in y direction to selectively implant dopants such as BF2 into the amorphous silicon film 32 coated on sidewall of the deep trench. It is noted that the tilt angle ion implantation process is performed only in y direction as specifically indicated in Fig.9, but not performed in x direction. Therefore, dopants are not implanted into the amorphous silicon film 32 in x direction.

[0034] As shown in Fig.11, an anisotropic etching is carried out to etch the amorphous silicon film 32 and the silicon oxide layer 31 deposited above the pad nitride layer 28 and

the amorphous silicon film 32 deposited at the bottom of the recess, thereby exposing the pad nitride layer 28 and Poly2. The remaining amorphous silicon film 32 and silicon oxide layer 31 form a spacer on sidewall of the deep trench.

[0035] As shown in Fig.12, a wet etching such as diluted ammonia solution is used to selectively etch away the non-doped portions (in x direction) of the remaining amorphous silicon film 32. The wet etching does not etch the doped portion (in y direction) of the amorphous silicon film 32. After the wet etching, the remaining portions of the amorphous silicon film 32 in y direction constitute a pair of symmetric spacers 33 on sidewall of the deep trench approximately above the collar oxide 15 and Poly2, thereby exposing the silicon oxide layer 31 in x direction. The exposed silicon oxide layer 31, which is not covered by the y-direction amorphous silicon spacers 33, is thereafter removed by using wet chemistry such as diluted HF, thereby exposing the silicon sidewalls in the deep trench in x direction. At this time, the surface of the y-direction amorphous silicon spacers 33, the exposed silicon sidewall, and the top surface of the collar oxide 15 and Poly2 constitute a new recess opening 42 at the top of the deep

trench capacitor.

[0036] As shown in Fig.13, a third polysilicon layer (Poly3) is deposited on the substrate and fills the recess opening 42. As shown in Fig.14, Poly3 and the y-direction amorphous silicon spacers 33 are then recessed to a predetermined depth, for example, 100~400 angstroms, below the surface of the substrate 10.

[0037] Please refer to Fig.15. Fig.15 is a schematic plane view showing the layout of the deep trench capacitors 11 after finishing the process steps through Fig.9 to Fig.14 and buried strap out diffusion process, wherein the perspective non-circular buried strap out diffusion regions 16 are also shown. As shown in Fig.15, since the amorphous silicon spacers 33 and the silicon oxide layer 31 covered by the amorphous silicon spacers 33 block the out diffusion path in y direction, the buried strap out diffusion regions 16 are only formed in x direction. This increases the process window when laying AA photo pattern. AA-DT misalignment is eliminated.

[0038] Those skilled in the art will readily observe that numerous modifications and alterations of the present invention may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as

limited only by the metes and bounds of the appended claims.